CLAIMS

What is claimed is:

Claim 1 (currently amended): A receive circuit comprising:

a. a data input terminal adapted to receive a stream of input data;

b. a first receive-circuit clock terminal adapted to receive a first clock signal;

c. a second receive-circuit clock terminal adapted to receive a second clock signal;

d. a first sampler having a first sampler data terminal coupled to the data input terminal, a first sampler clock terminal coupled to the first receive-circuit clock terminal, and a first data output terminal;

e. a second sampler having a second sampler data terminal coupled to the data input terminal, a second sampler clock terminal coupled to the second receive-circuit clock terminal, and a second data output terminal; and

f. a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node.

Claim 2 (original): The receive circuit of claim 1, wherein the data input terminal, the first sampler, the second sampler, and the comparison circuit are disposed on a semiconductor chip.

Claim 3 (original): The receive circuit of claim 1, wherein the first and second samplers sample the stream of input data to produce respective first and second sampled-data streams,

and wherein the comparison circuit is adapted to compare at least one of the sampled-data streams with expected data.

Claim 4 (original): The receive circuit of claim 1, wherein the comparison circuit issues an error signal in response to mismatches between the first and second sampled-data streams.

Claim 5 (original): The receive circuit of claim 4, wherein the comparison circuit issues an error signal in response to each mismatch between the first and second sampled-data streams.

Claim 6 (currently amended): The receive circuit of claim 1, further comprising clock control circuitry coupled to the second receive-circuit clock terminal and providing the second clock signal, wherein the clock control circuitry is adapted to vary the phase of the second clock signal in response to a timing control signal.

Claim 7 (original): The receive circuit of claim 6, wherein the clock control circuitry varies the phase of the first clock signal in response to a second timing control signal.

Claim 8 (currently amended): The receive circuit of claim 1, further comprising a third sampler having a third sampler data terminal coupled to the data input terminal, a third sampler clock terminal, and a third data output terminal.

Claim 9 (original): The receive circuit of claim 8, further comprising a multiplexer having a first multiplexer input

terminal coupled to the first data output terminal, a second multiplexer input terminal connected to the third data output terminal, a select terminal, and a multiplexer output terminal.

Claim 10 (original): The receive circuit of claim 9, wherein the first multiplexer input terminal is coupled to the first data output terminal via the comparison circuit.

Claim 11 (original): The receive circuit of claim 9, wherein the first comparison circuit input node is coupled to the multiplexer output terminal and the first multiplexer input terminal is coupled to the first data output terminal.

Claim 12 (original): A method comprising:

a. sampling a series of input symbols using a first clock signal of a first clock phase to produce a first series of sampled symbols;

b. sampling the series of input symbols using a second clock signal of a second clock phase to produce a second series of sampled symbols; and

c. comparing sampled symbols of the first series of sampled symbols with corresponding sampled symbols of the second series of sampled symbols.

Claim 13 (original): The method of claim 12, further comprising adjusting, in response to the comparing, at least one of the first and second clock phases with respect to the other of the first and second clock phases.

Claim 14 (original): The method of claim 12, wherein the sampling and comparing are completed on a semiconductor chip.

Claim 15 (currently amended): The method of claim 12, wherein the series of input symbols are sampled using the first clock phase at a first sample voltage and ~~the~~ using the second clock phase at a second sample voltage.

Claim 16 (original): The method of claim 15, further comprising adjusting at least one of the first and second sample voltages with respect to the other of the first and second sample voltages in response to the comparing.

Claim 17 (original): The method of claim 12, further comprising issuing an error signal in response to a mismatch between ones of the first and second series of sampled symbols.

Claim 18 (original): The method of claim 12, wherein the comparing produces error data for a plurality of phase offsets between the first and second clock phases, the method further comprising storing the error data.

Claim 19 (original): The method of claim 18, further comprising storing information regarding each of the phase offsets and the corresponding error data.

Claim 20 (original): The method of claim 18, further comprising calculating a timing margin using the error data.

Claim 21 (currently amended): The method of claim 18, wherein the series of input symbols are sampled using the first clock

phase at a first sample voltage and ~~the~~ using the second clock phase at a second sample voltage, and wherein the comparing produces second error data for a plurality of voltage offsets between the first and second sample voltages.

Claim 22 (original): The method of claim 21, further comprising plotting the first-mentioned error data and the second error data.

Claim 23 (original): A method comprising:

a. sampling a series of data symbols using a first sample voltage to produce a first series of sampled-data symbols;

b. sampling the series of data symbols using a second sample voltage to produce a second series of sampled-data symbols; and

c. comparing corresponding ones of the first and second series of sampled-data symbols.

Claim 24 (original): The method of claim 23, further comprising adjusting at least one of the first and second sample voltages with respect to the other of the first and second sample voltages.

Claim 25 (original): The method of claim 23, wherein the sampling and comparing are completed on a semiconductor chip.

Claim 26 (original): The method of claim 23, wherein the series of data symbols are sampled using a first clock signal of a

first clock phase and using a second clock signal of a second clock phase.

Claim 27 (original): The method of claim 26, further comprising adjusting at least one of the first and second clock phases with respect to the other of the first and second clock phases in response to the comparing.

Claim 28 (original): The method of claim 27, further comprising storing information regarding the first and second sample voltages and the first and second clock phases.

Claim 29 (original): The method of claim 28, further comprising calculating a timing margin using the information.

Claim 30 (original): The method of claim 29, further comprising plotting the information.

Claim 31 (original): The method of claim 23, wherein comparing corresponding ones of the first and second series of sampled-data symbols includes comparing only a subset of the first and second series of sampled-data symbols.

Claim 32 (original): The method of claim 23, further comprising matching the first series of sampled-data symbols to at least one data pattern.

Claim 33 (original): The method of claim 32, wherein the comparing corresponding ones of the first and second series of sampled-data signals occurs when the matching produces a match.

Claim 34 (original) A communication system comprising:

a. a transmitter adapted to transmit a series of data symbols; and

b. a receive circuit including:

c. a data input terminal adapted to receive the series of data symbols;

d. a first clock node adapted to receive a first clock signal;

e. a second clock node adapted to receive a second clock signal;

f. a first sampler having a first sampler data terminal coupled to the data input terminal, a first sampler clock terminal coupled to the first clock node, and a first data output terminal;

g. a second sampler having a second sampler data terminal coupled to the data input terminal, a second sampler clock terminal coupled to the second clock node, and a second data output terminal; and

h. a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node.

Claim 35 (original): The communication system of claim 34, wherein the first and second samplers and the comparison circuit are disposed on a first semiconductor chip.

Claim 36 (original): The communication system of claim 35, wherein the transmitter is disposed on a second semiconductor chip.

Claim 37 (original): The communication system of claim 34, wherein the receive circuit further includes an error filter having a first error-filter input terminal coupled to at least one of the first and second sampler output terminals and a second error-filter input terminal coupled to the comparison-circuit output node.

Claim 38 (original): The communication system of claim 37, wherein the error filter includes a pattern-matching circuit that compares sampled data from the first data output terminal with a data pattern.

Claim 39 (original): The communication system of claim 38, wherein the error filter conveys sampled error symbols on the comparison-circuit output node when the sampled data matches the data pattern.

Claim 40 (original): A receiver comprising:

a. a data input terminal adapted to receive a stream of input data;

b. a first clock node adapted to receive a first clock signal;

c. a second clock node adapted to receive a second clock signal;

d. first sampling means having a first sampler data terminal coupled to the data input terminal, a first

clock terminal coupled to the first clock node, and a first data output terminal;

e. second sampling means having a second sampler data terminal coupled to the data input terminal, a second clock terminal coupled to the second clock node, and a second data output terminal; and

f. error-detection means coupled to the first and second data output terminals.

Claim 41 (original): The receiver of claim 40, wherein the first and second sampling means sample the stream of input data to produce respective first and second sampled-data streams.

Claim 42 (original): The receiver of claim 41, wherein the comparison circuit issues an error signal in response to mismatches between the first and second sampled-data streams.

Claim 43 (original): The receiver of claim 42, wherein the comparison circuit issues an error signal in response to each mismatch between corresponding data symbols in the first and second sampled-data streams.

Claim 44 (original): The receiver of claim 41, further comprising a data filter having a first data-filter input terminal coupled to at least one of the first and second sampler output terminals and a second data-filter input terminal coupled to the comparison-circuit output node.

Claim 45 (original): The receiver of claim 44, wherein the data filter includes a pattern-matching means for comparing

sampled data from the first data output terminal with a data pattern.

Claim 46 (original): The receiver of claim 45, wherein the data filter conveys sampled data symbols on the comparison-circuit output node when the sampled data matches the data pattern.

CONCLUSION

Claims 1-46 are pending in the above-identified application.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on: Oct. 26, 2004

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